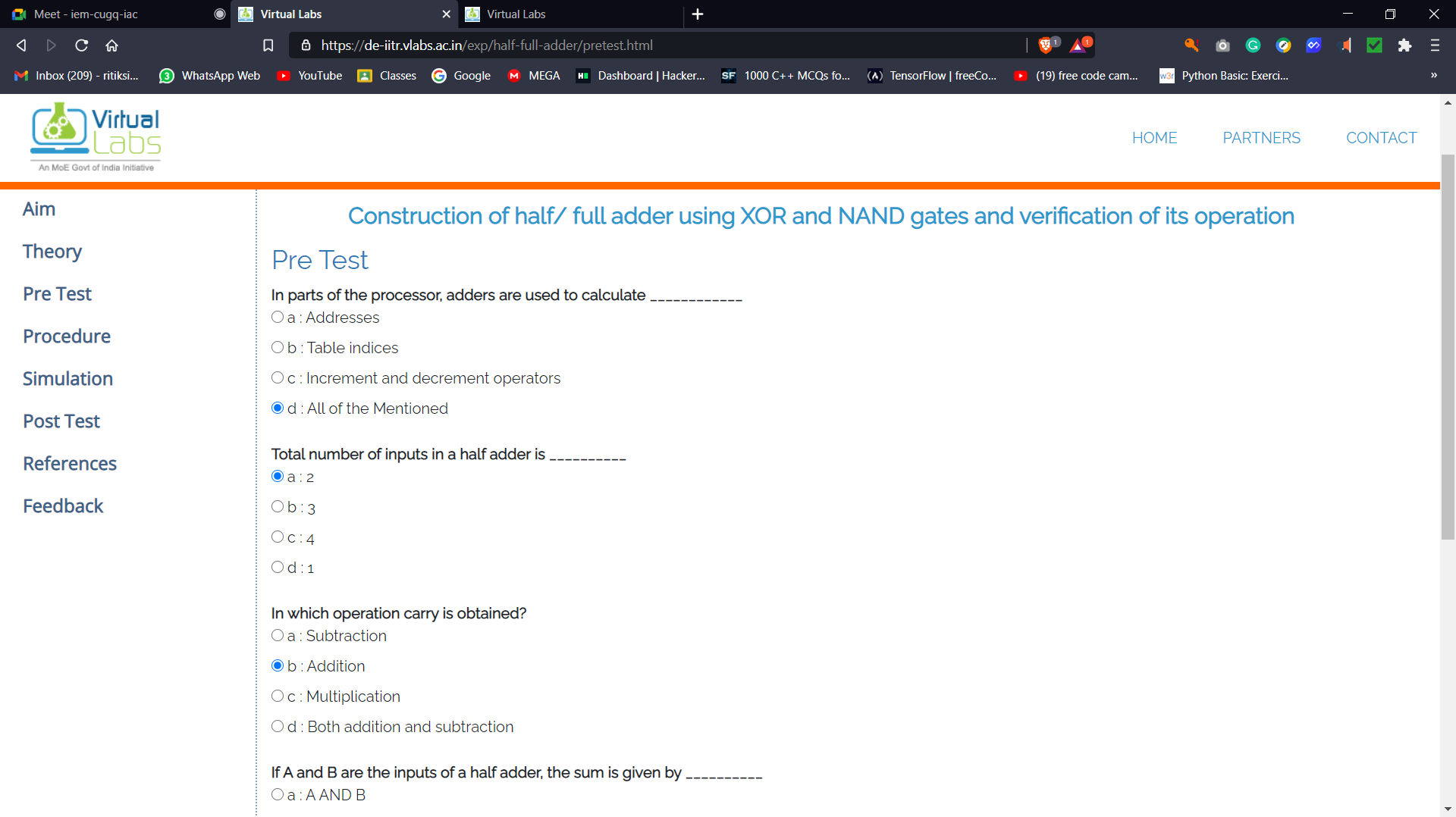
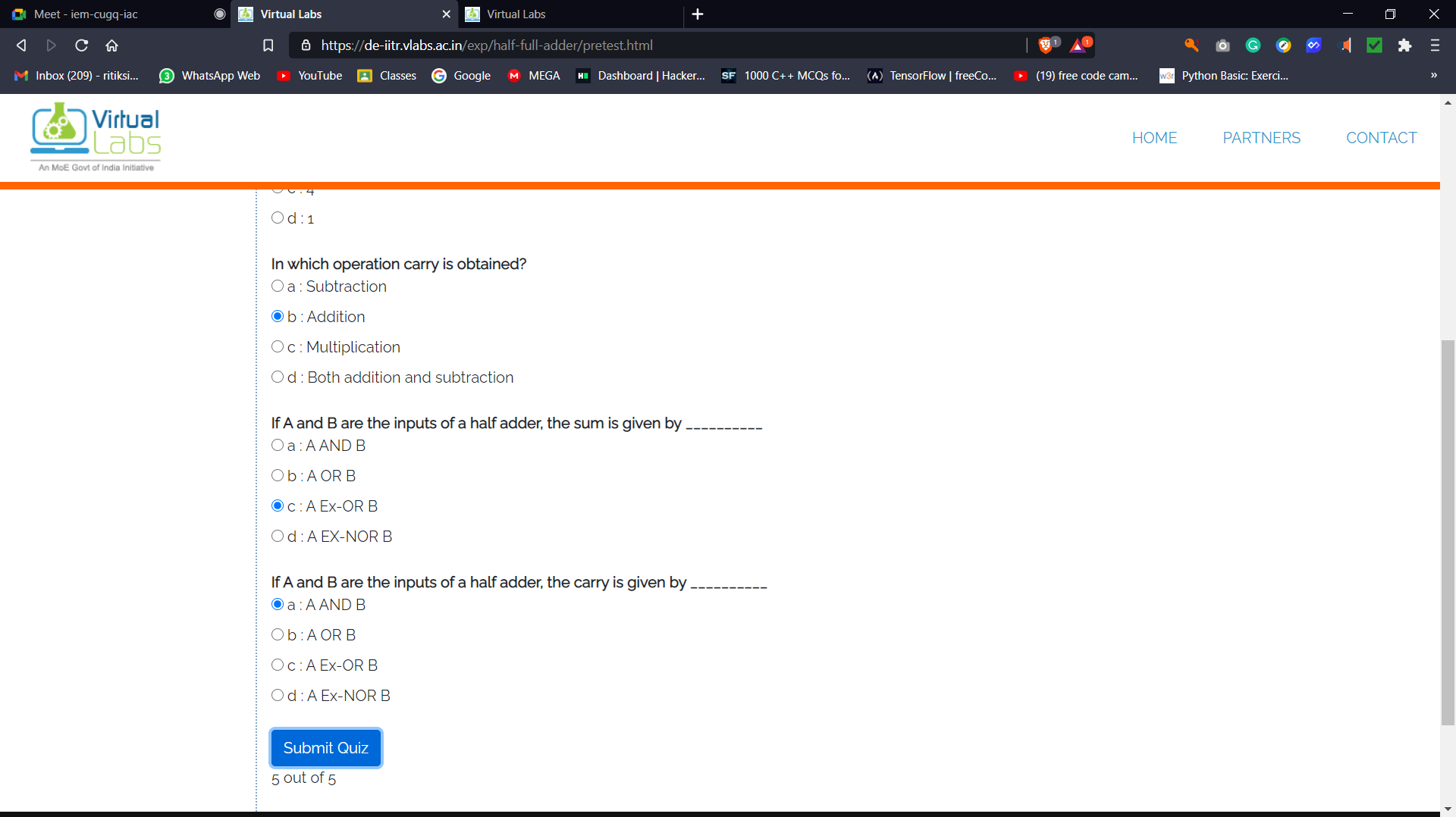
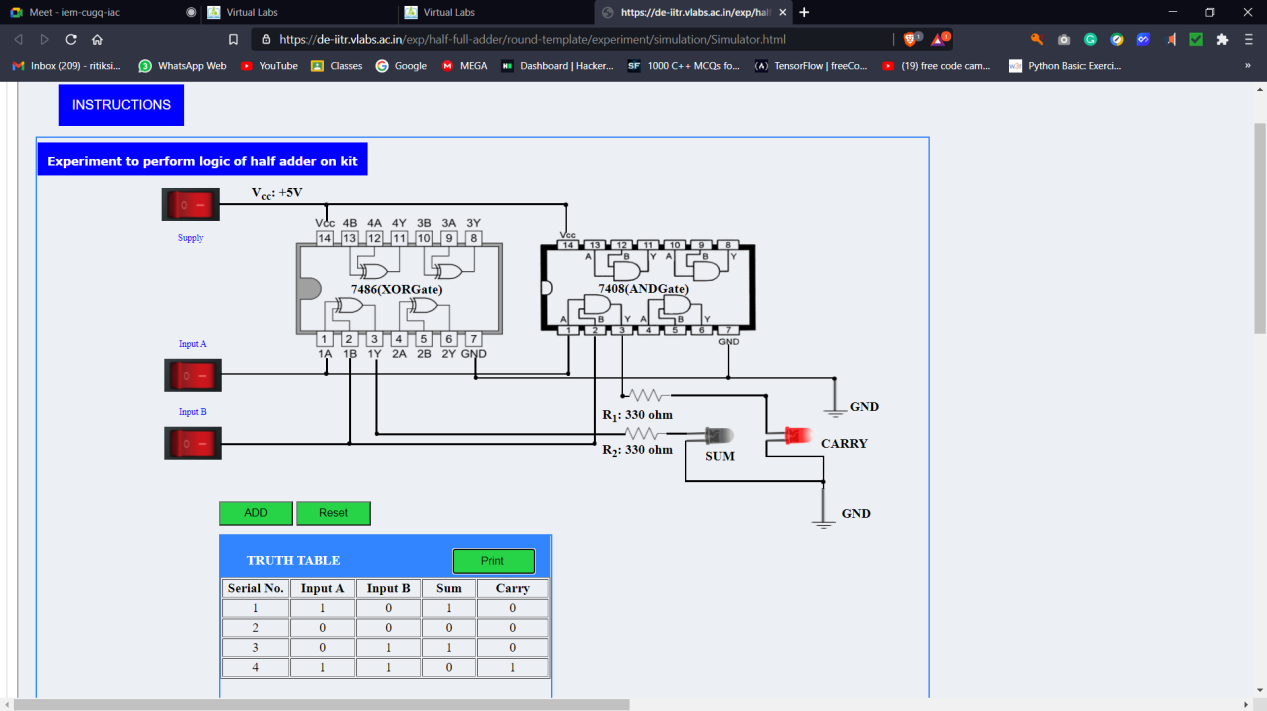
## **Construction of half/ full adder using XOR and NAND gates and verification of its operation**

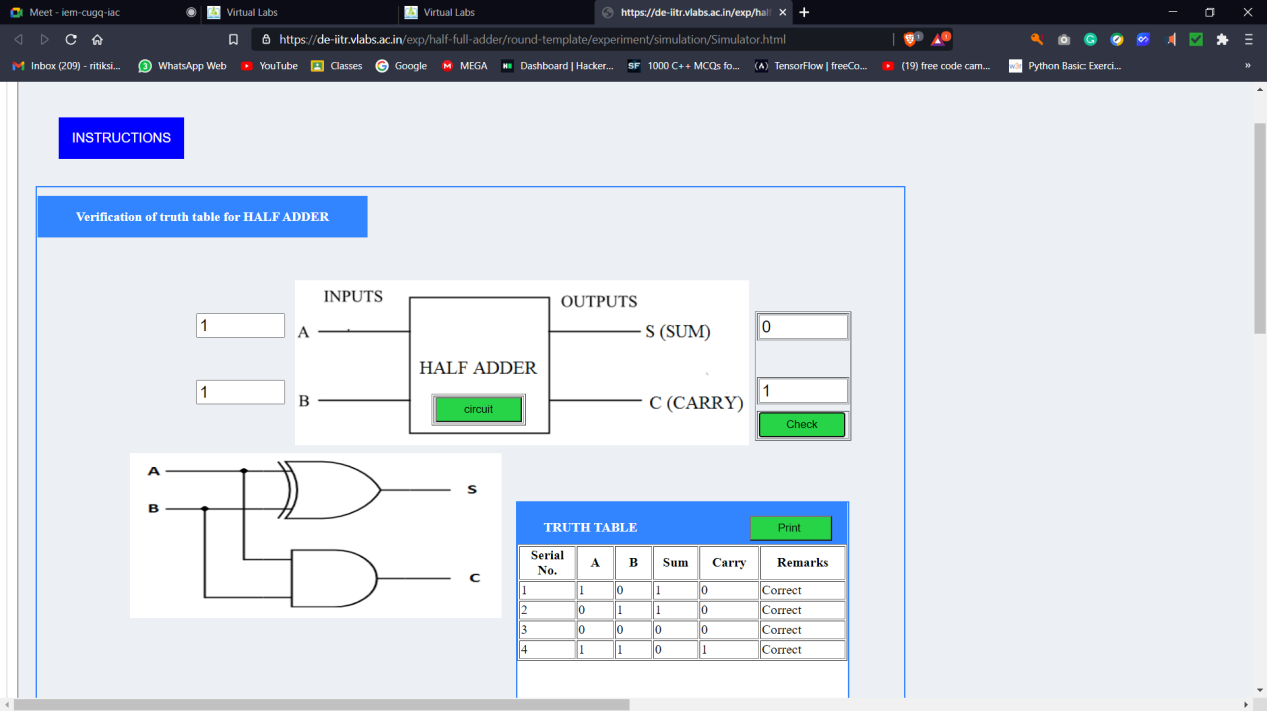
**PRE TEST**



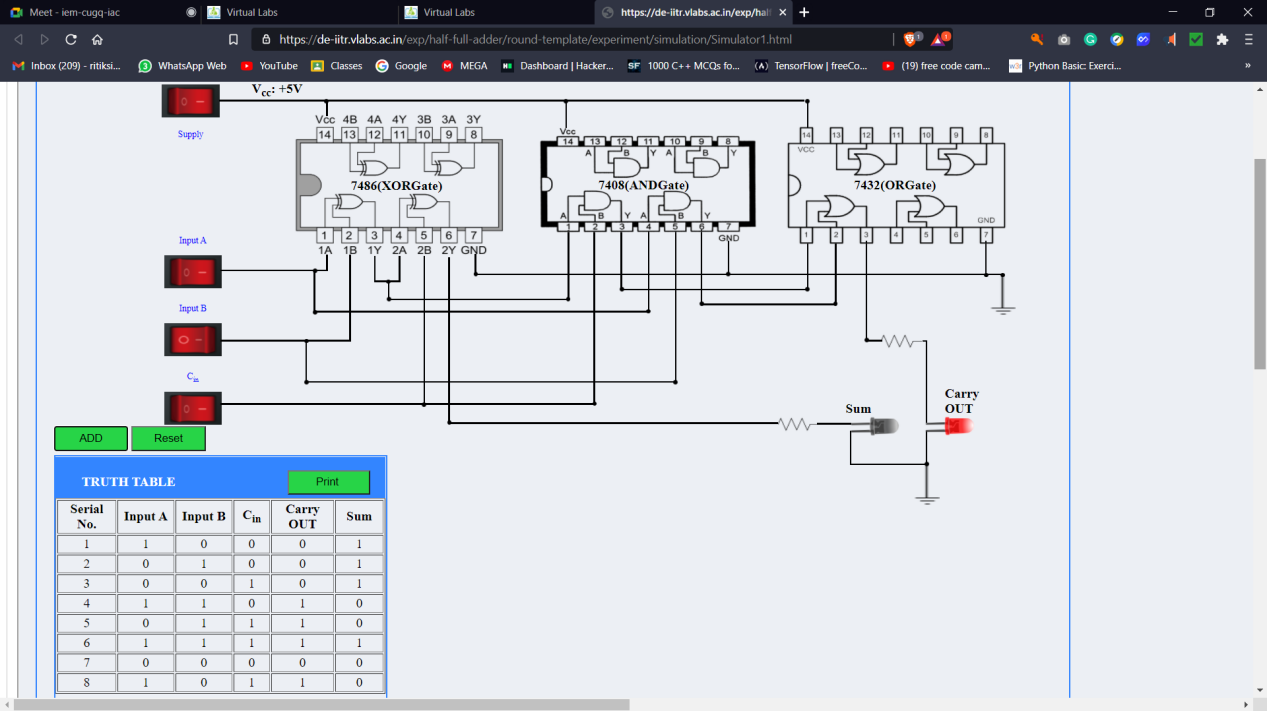


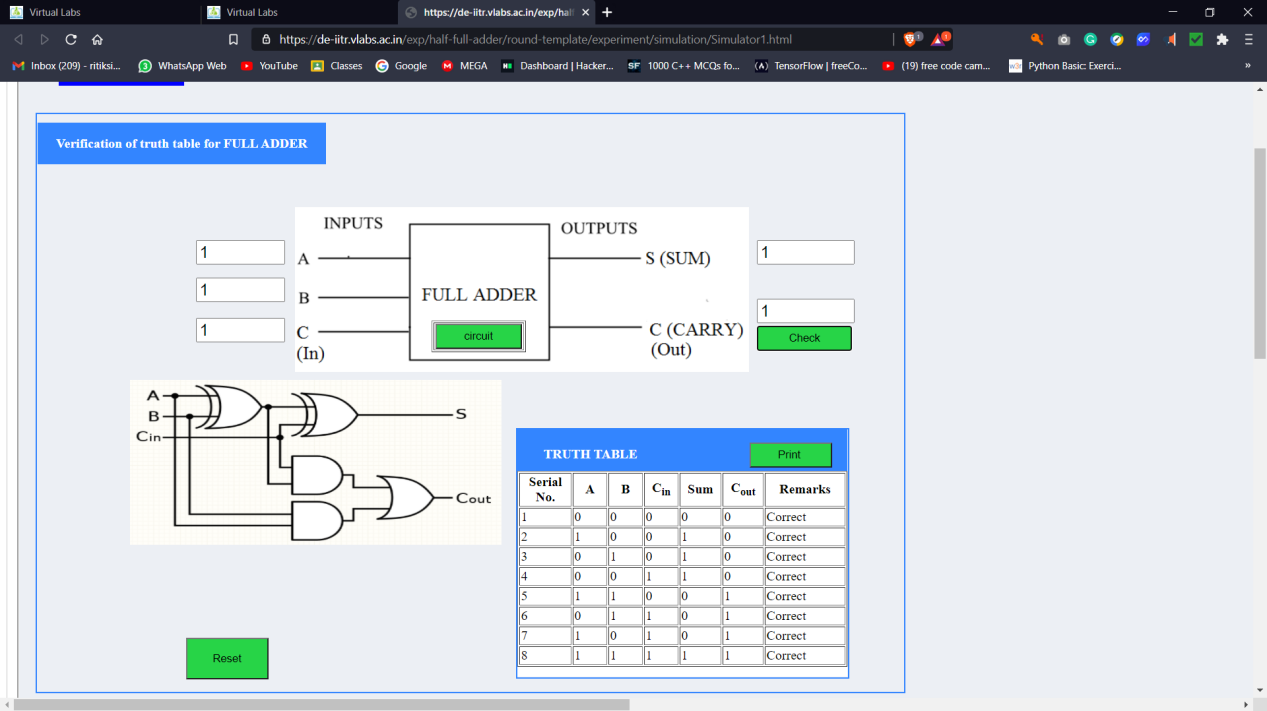
**HALF ADDER**



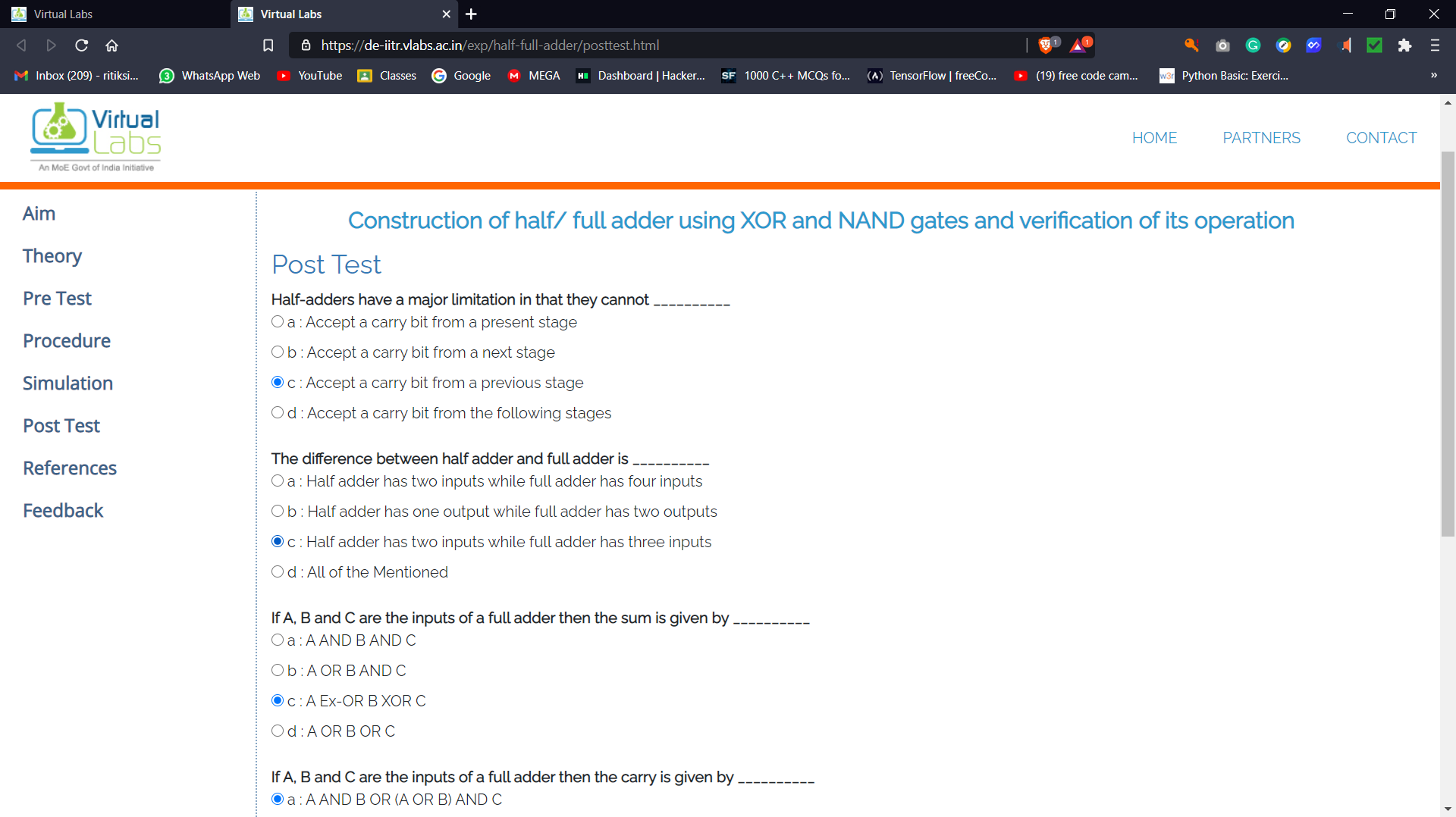


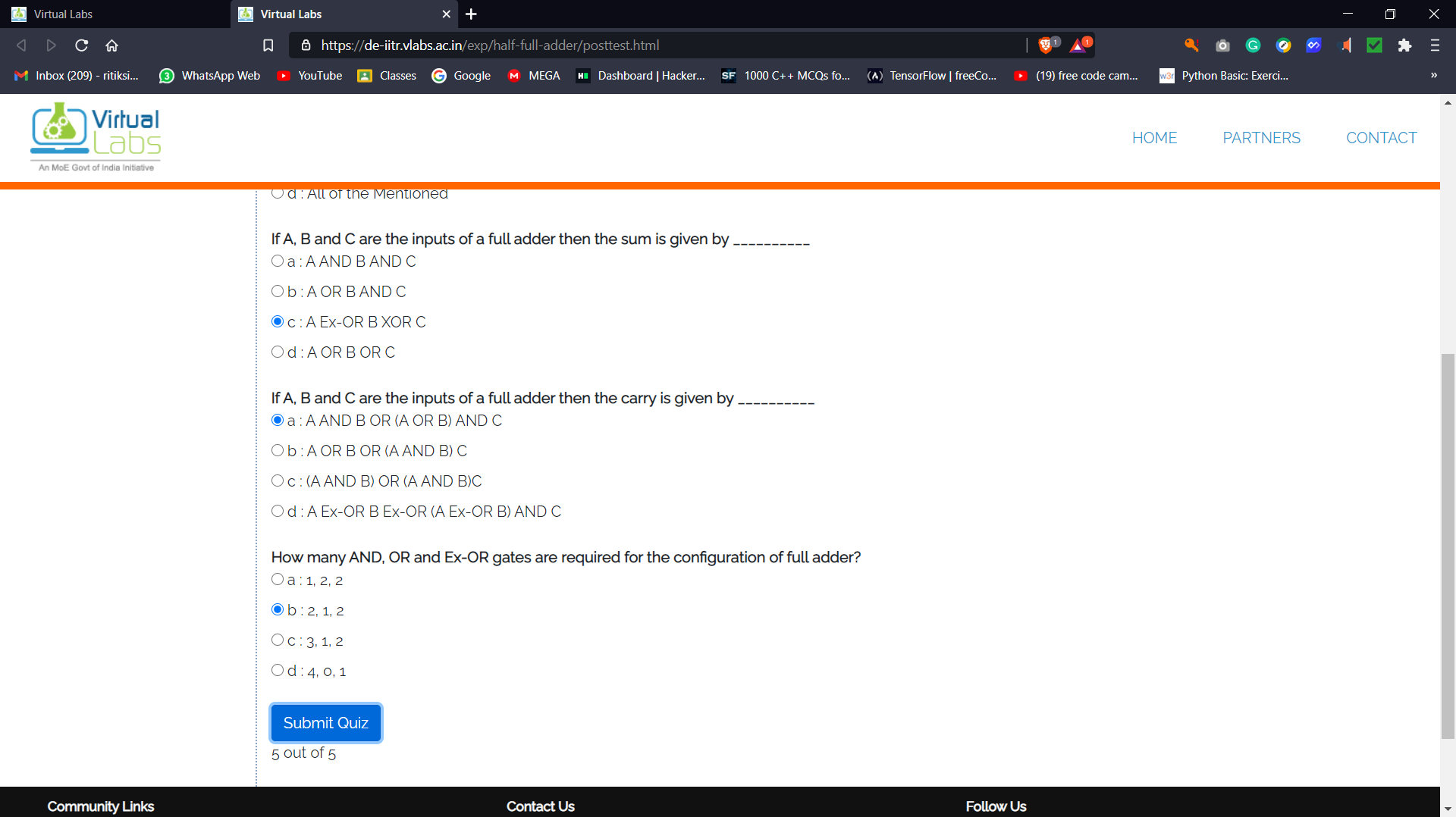
**FULL ADDER**

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**POST TEST**

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